Very low thermal drift precision virtual voltage reference

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P. S. Crovetti

A digital-based, process-supply-and-temperature (PVT) independent voltage reference suitable to nanoscale CMOS technologies, which exploits the recently proposed *virtual reference* concept to achieve a very low thermal drift, is presented in this Letter. Its performance is assessed on the basis of simulations and experiments carried out on a microcontroller-based, proof-of-concept prototype and is compared with state-of-the-art integrated analog and digital voltage references. A simulated (measured) thermal drift as low as $1\mathrm{ppm}/^\circ\mathrm{C}$ ($5\mathrm{ppm}/^\circ\mathrm{C}$) in the temperature range $-40/+140^\circ\mathrm{C}$ ($-10/+100^\circ\mathrm{C}$) is reported.

Introduction: Accurate reference voltages, which are needed in present-day integrated systems, are normally generated by analog cells designed so that their output is constant and as independent as possible of process parameters, power supply voltage and temperature (PVT-independent).

Traditional bandgap references [1], however, are not suitable to present-day low voltage, nano-scale CMOS technologies and even though several low voltage alternatives have been proposed [2, 3], the design of accurate, low thermal drift references in advanced CMOS technologies is still challenging because of the poor analog characteristics of nano-scale devices. Addressing the limitations of analog voltage references, the digital *virtual reference* concept has been recently proposed in [4] and its advantages in terms of accuracy, power consumption and silicon area occupancy have been discussed.

In this Letter, a digital virtual voltage reference based on a novel algorithm, specifically devised to achieve a very low thermal drift, is presented and its effectiveness is verified by computer simulations and measurements carried out on a microcontroller-based prototype.

Virtual Voltage Reference Concept: The virtual reference approach is intended to provide an accurate, PVT-independent voltage reference in a System-on-Chip (SoC), which is based on a digital core and includes an N-bit A/D converter (ADC) and an N-bit D/A converter (DAC), both referenced to a possibly non-PVT independent *pseudo-reference* V_0, as shown in Fig.1a. The pseudo-reference V_0 is only assumed to be constant within one least significant bit (LSB) for a conveniently long time and can be obtained sampling an inaccurate power supply voltage by a sample-and-hold circuit. In this framework, a binary integer r, so that the voltage v_{REF} resulting from its D/A conversion by the V_0-referenced DAC in the SoC, i.e.

$$v_{\mathrm{REF}} = r\frac{V_0}{2^N}, \tag{1}$$

is constant and PVT-independent within 1 LSB regardless of variations in V_0, is defined as a *virtual voltage reference*. On the basis of r in (1), in fact, since $V_0 = v_{\mathrm{REF}}\frac{2^N}{r}$, signal samples acquired by the V_0-referenced ADC of the SoC can be digitally translated into v_{REF}-referenced samples by multiplication by $\frac{2^N}{r}$. Moreover, a PVT-independent physical reference voltage can be obtained by D/A-conversion of (an integer proportional to) the virtual reference r by the V_0-referenced DAC in the SoC. The virtual reference r can be therefore regarded as a full replacement of a physical reference voltage.

An estimate of the virtual reference r appearing in (1) can be obtained in the SoC of Fig.1a by the procedure outlined in Fig.1b. To this purpose, a pn diode D is introduced in the SoC of Fig.1a as a *physical standard* and it is operated under different bias conditions $i = 1 \ldots M$, via the resistor R, by the DAC output. The diode forward voltages $v_{\mathrm{D}}^{(i)}$ corresponding to the different bias conditions (*voltage primitives*) are then acquired by the ADC and the virtual reference r is evaluated by processing the acquired digital samples $n^{(i)}$ of the voltage primitives $v_{\mathrm{D}}^{(i)}$, so that to implement the functional equivalent of analog references in the digital domain, as illustrated in [4].

In order to avoid the dependance of the voltage primitives on the pseudo-reference V_0, the procedure described so far is iterated biasing the physical standard D/A-converting digital values proportional to the virtual reference r at the previous iteration, until the estimates of r in two next iterations are equal within a tolerance ε. In practice, the procedure

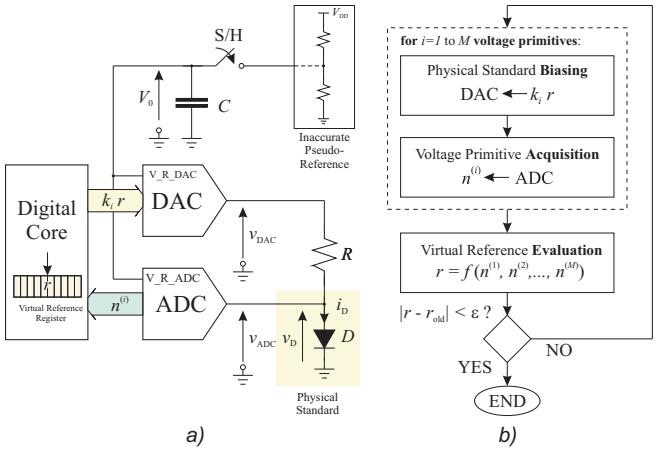

Fig. 1 *A virtual voltage reference in a mostly digital SoC: a) hardware platform, b) PVT-compensation software procedure.*

in Fig.1b, needs to be repeated only once in a second or more and can be implemented in a SoC with a minimum performance overhead.

In the following, the virtual reference approach introduced so far is extended and a novel virtual reference evaluation procedure, which has not an analog counterpart, is proposed to achieve a very low thermal drift.

Novel Virtual Voltage Reference Evaluation Procedure: With reference to the SoC architecture in Fig.1a, the novel virtual voltage reference evaluation procedure is based on two voltage primitives v_1 and v_2, to be acquired by the ADC in Fig.1a, which show different functional dependencies $f(\cdot)$ and $g(\cdot)$ on the absolute temperature T, i.e. $v_1 = f(T)\cdot V_{\mathrm{u}}$ and $v_2 = g(T)\cdot V_{\mathrm{u}}$, where $V_{\mathrm{u}} = 1\mathrm{V}$ is a unitary voltage. Assuming that $g(\cdot)$ is invertible and being $g^{-1}(\cdot)$ its inverse, the temperature T can be expressed in terms of v_2 as

$$T = g^{-1}\left(\frac{v_2}{V_{\mathrm{u}}}\right) \tag{2}$$

Hence, replacing (2) in the expression of v_1, a functional relation between the voltage primitives v_1 and v_2 at the same temperature T in the form

$$\frac{v_1}{V_{\mathrm{u}}} = f\left[g^{-1}\left(\frac{v_2}{V_{\mathrm{u}}}\right)\right] = \tilde{f}\left(\frac{v_2}{V_{\mathrm{u}}}\right) \tag{3}$$

can be established so that the condition

$$\frac{v_1}{V_{\mathrm{u}}} - \tilde{f}\left(\frac{v_2}{V_{\mathrm{u}}}\right) = 0 \tag{4}$$

is identically verified at any temperature for any (v_1, v_2) pair. Neglecting quantization and other ADC errors, the voltages v_1 and v_2 appearing in (4) can be expressed in terms of their samples n_1, n_2, acquired by the V_0-referenced ADC in Fig.1a as $v_1 = \frac{n_1}{2^N}V_0$ and $v_2 = \frac{n_2}{2^N}V_0$. By replacing such expressions in (4), one gets

$$\alpha n_1 - \tilde{f}(\alpha n_2) = 0 \tag{5}$$

which can be regarded as an equation in the unknown $\alpha = \frac{V_0}{2^N V_{\mathrm{u}}}$ involving the pseudo-reference V_0. Assuming that (5) has a unique solution $\alpha = \alpha^\star$, it follows that

$$V_{\mathrm{u}} = \frac{1}{\alpha^\star}\frac{V_0}{2^N}. \tag{6}$$

By comparing (6) and (1), being V_{u} constant by definition, the reciprocal of the solution $\alpha^\star$ of (5) can be considered as a virtual voltage reference.

Provided that the relation $\tilde{f}(\cdot)$ between voltages v_1 and v_2 at the same temperature T is accurately known, equation (5) can be numerically solved by the digital core in Fig.1 to evaluate the virtual reference r in (1) from the samples n_1 and n_2 of the primitives acquired by the ADC.

Virtual Voltage Reference Design and Simulation: A virtual reference implementing the technique proposed so far has been designed in a 180nm, 1.8V-supply CMOS technology. Such a reference is based on the hardware platform of Fig.1a, including an ADC and a DAC with a resolution $N = 16\mathrm{bit}$ and a n+-p well $20\mu\mathrm{m} \times 20\mu\mathrm{m}$ junction diode D biased by a poly resistor $R = 23\,\mathrm{k}\Omega$ as a physical standard. The voltages

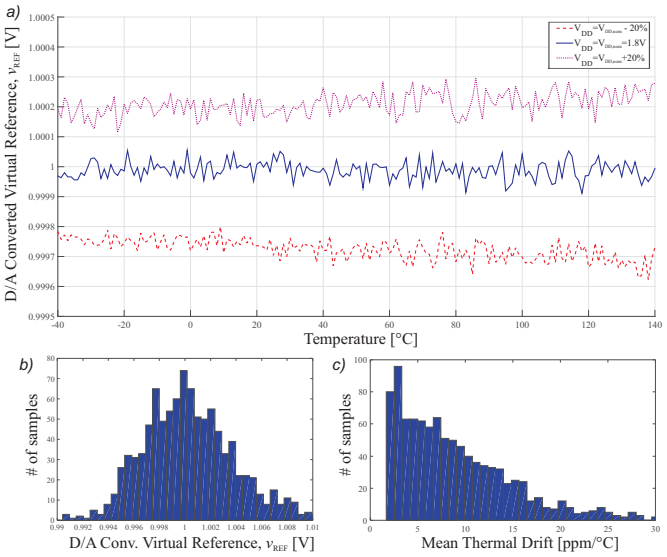

Fig. 2 *Proposed virtual reference simulated performace: a) D/A-converted virtual reference against temperature for* $1.8\text{V} \pm 20\%$ *power supply; b) distribution of the D/A-converted virtual reference over process variations (Montecarlo simulations); c) distribution of the D/A-converted virtual reference thermal drift over process variations (Montecarlo simulations).*

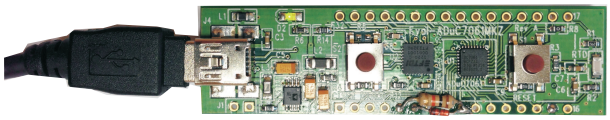

Fig. 3. Photograph of the microcontroller-based proof-of-concept prototype.

$v_1(T) = v_{\text{D}}^{(1)}$ and $v_2(T) = v_{\text{D}}^{(1)} - v_{\text{D}}^{(2)}$, being $v_{\text{D}}^{(1)}$ and $v_{\text{D}}^{(2)}$ the diode D forward voltages under two different bias conditions (corresponding to a nominal bias current of 40μA and 20μA, respectively) defined independently of the power supply as in Fig.1b, are considered as voltage primitives. The relation $\tilde{f}(\cdot)$ between v_1 and v_2 appearing in (5) has been modeled by a 6^{th}-order polynomial, whose coefficients have been extracted fitting experimental data by the least-mean-squares method.

The operation of the virtual voltage reference has been simulated on the basis of accurate experimentally validated models of the diode D and of the resistor R from the silicon foundry, as in [4]. In Fig.2 the simulated thermal drift of the D/A converted virtual reference is reported for a supply voltage of $1.8V \pm 20\%$. A mean drift (box method) of less than $1\,\text{ppm}^\circ\text{C}$ in the temperature range $-40/+140^\circ\text{C}$ can be observed. The line regulation at ambient temperature is about $0.04\%/\text{V}$.

Moreover, the performance of the proposed virtual reference over process variations has been tested by Montecarlo simulations (1,000 runs) and the statistical distributions of the D/A-converted virtual reference and of its thermal drift are reported in Fig.2b and in Fig.2c, respectively. Based on such simulations, the standard deviation of the untrimmed reference voltage at ambient temperature is less than 3.8mV, the mean value of the thermal drift over process spreads is $9.3\,\text{ppm}^\circ/\text{C}$ and its standard deviation is $6.7\,\text{ppm}^\circ/\text{C}$.

Microcontroller-Based Prototype and Experiments: The virtual voltage reference prototype in Fig.3, which is based on the MiniKit evaluation board of the ADuC7061 microcontroller by Analog Devices and includes an external 1N4148 junction diode biased by a $10\text{k}\Omega$ resistor as a physical standard, has been developed to validate the novel low thermal drift compensation technique presented in this Letter. In such a prototype, the microcontroller has been programmed to evaluate the virtual reference as discussed above, using a polynomial approximation of the function $\tilde{f}(\cdot)$ in (5) based on an experimental characterization of the diode D.

The D/A-converted virtual reference obtained from the prototype has been measured over temperature as described in [4] and measured results are plotted in Fig.4. Such results show that the D/A converted virtual reference, whose nominal value is 1.623V, has a residual thermal drift of less than $5\text{ppm}/^\circ\text{C}$ in the temperature range from $-10/+100^\circ\text{C}$. Such a drift is low, but larger than in simulations because the estimate of $\tilde{f}(\cdot)$ in (5) is now affected by measurement errors, to be addressed in future work. Finally, the measured line regulation of the prototype is 0.2%/V and the measured root-mean-square (rms) noise is about $130\mu\text{V}$.

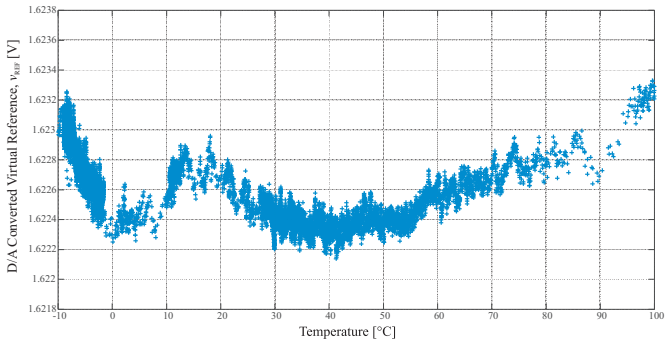

Fig. 4 *Measured thermal drift of the D/A-converted virtual reference of the microcontroller-based proof-of-concept prototype.*

Table 1: Voltage Reference Circuits Performance Comparison

Reference	[2]	[3]	[4]		This Work	
Technology, μm	0.18	0.13	0.18	PCB	0.l8	PCB
Min. Supply, V	1.2	1.2	0.9	2.4	0.9	2.4
Analog/Digital	An.	An.	Dig.	Dig.	Dig.	Dig.
Characterization	Meas.	Meas.	Sim.	Meas.	Sim.	Meas.
Ref. Volt., V	0.767	0.735	1.000	1.157	1.000	1.623
ADC/DAC # bit	N/A	N/A	16	16	16	16
Untrimm. Accuracy Std. Dev., mV, %	N/A	~ 10 $\sim 1.5\%$	1.4 0.14%	N/A	3.8 0.38%	N/A
Temp. Range, °C	-40 +120	-40 +120	-40 +140	-10 100	-40 +140	-10 100
Nominal Temp. Coeff., ppm/°C	4.5	4.2	7	16	1	5
Untrimm. TC, Avg., ppm/°C	5	9.3	8.7	N/A	9.3	N/A
Untrimm. TC, Std. Dev., ppm/°C	1.5	4.8	1.7	N/A	6.7	N/A
Line Reg., $\%/V$	1	0.5	0.02	0.15	0.04	0.15
Silicon Area, μm^2	36,000	63,000	700	N/A	2,000	N/A
Power, μW	43	144	0.12	N/A	0.48	N/A

Comparison and Benchmarking: The performance of the virtual voltage references proposed in this Letter is compared in Tab.1 with recently proposed analog voltage references [2, 3] and with the digital virtual references proposed in [4]. The virtual references presented in this Letter show a very low thermal drift which is in line with best analog references and better than previously proposed digital references, even though their untrimmed performance is slightly worse. Moreover, the silicon area overhead and the power consumption of the proposed references are both much lower than in analog references.

Conclusion: A digital virtual voltage reference, based on a novel evaluation algorithm devised to achieve a very low thermal drift, has been presented in this Letter. A simulated (measured) thermal drift of $1\text{ppm}/^\circ\text{C}$ ($5\text{ppm}/^\circ\text{C}$) in the temperature range $-40/+140^\circ\text{C}$ ($-10/+100^\circ\text{C}$), better than previously proposed digital references, has been reported by computer simulations and experiments carried out on a microcontroller-based, proof-of-concept prototype.

P. S. Crovetti, *Dept. of Electronics and Telecommunications (DET), Politecnico di Torino, Torino, Italy*

E-mail: paolo.crovetti@polito.it

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